



EB13C5 C 1 H -16.000M

Series — RoHS Compliant (Pb-free) Low Current 3.3V 4 Pad 3.2mm x 5mm Ceramic SMD LVCMOS Oscillator

Frequency Tolerance/Stability -±100ppm over 0°C to +70°C Nominal Frequency 16.000MHz Logic Control / Additional Output Tri-State

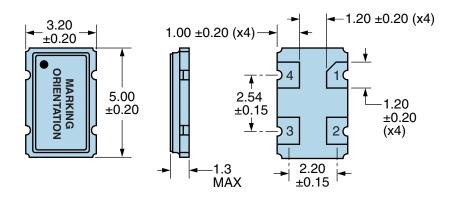
Duty Cycle -50 ±10%

ELECTRICAL SPECIFICATIONS				
16.000MHz				
±100ppm over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Ouput Load Change, First Year Aging at 25°C, Shock, and Vibration)				
3.3Vdc ±10%				
3mA Maximum				
90% of Vdd Minimum				
-1.6mA				
10% of Vdd Maximum				
+1.6mA				
6nSec Maximum (Measured at 20% to 80% of waveform)				
50 ±10% (Measured at 50% of waveform)				
15pF Maximum				
CMOS				
Tri-State Tri-State				
90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)				
10μA Maximum (Disabled Output: High Impedance)				
25pSec Maximum				
10 mSec Maximum				
-55°C to +125°C				

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS				
Fine Leak Test	MIL-STD-883, Method 1014, Condition A			
Gross Leak Test	MIL-STD-883, Method 1014, Condition C			
Mechanical Shock	MIL-STD-202, Method 213, Condition C			
Resistance to Soldering Heat	MIL-STD-202, Method 210			
Resistance to Solvents	MIL-STD-202, Method 215			
Solderability	MIL-STD-883, Method 2003			
Temperature Cycling	MIL-STD-883, MEthod 1010			
Vibration	MIL-STD-883, Method 2007, Condition A			



MECHANICAL DIMENSIONS (all dimensions in millimeters)



PIN	CONNECTION
1	Tri-State
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E16.000 E=Ecliptek Designator
2	XXYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

Suggested Solder Pad Layout

All Dimensions in Millimeters



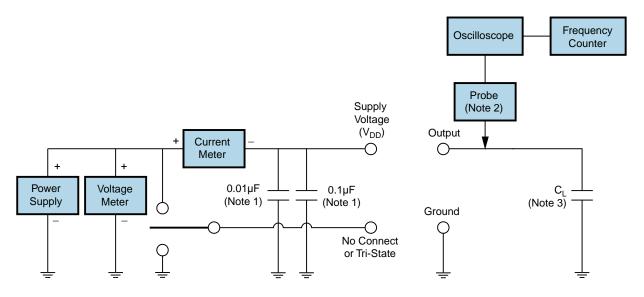
All Tolerances are ±0.1



OUTPUT WAVEFORM & TIMING DIAGRAM



Test Circuit for CMOS Output



- Note 1: An external $0.1\mu\text{F}$ low frequency tantalum bypass capacitor in parallel with a $0.01\mu\text{F}$ high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value \dot{C}_L includes sum of all probe and fixture capacitance.



Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T _s MAX to T _∟ (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _S MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T _L to T _P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T _P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T _P Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1



Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T _S MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	N/A
- Temperature Typical (T _S TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	60 - 120 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	240°C Maximum
Target Peak Temperature (T _P Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.